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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,921	12/10/2001	Robert Thomas Bailis	RPS920010132US1	5851

47052 7590 03/29/2005

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,921	BAILIS ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

In pages 1-2, the blank spaces in the CROSS RELATED APPLICATIONS section should be filled/updated with serial numbers and patent numbers if patented.

Claim Objections

Claims 1, 3, 5-6, 8, 10 are objected to because "can be" and "can" are not positive recitation of the invention and should not be used in the claim language.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Payne et al (USP 6347395)

(Claim 1) a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions (fig 1-3); and

at least one FPGA cell, coupled to the plurality of peripheral functions, wherein the FPGA cell [can be] is configured to selectively enable the plurality of peripheral functions (fig 1-3).

(Claims 6-7) a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions (fig 1-3);

a plurality of buses (in fig 1-5) wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB); and

a plurality of FPGA cells (fig 1-3), each of the plurality of FPGA cells coupled to a portion of the peripheral functions and to one of the plurality of buses, wherein each of the plurality of FPGA cells [can be] is configured to selectively enable a number of peripheral functions (fig 1-3).

(Claim 10) a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions (fig 1-3);

a plurality of buses (in fig 1-5), wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB), and

a plurality of FPGA cells (fig 1-3), each of the plurality of FPGA cells coupled to a portion of the peripheral functions and to one of the plurality of buses, wherein each of the plurality of FPGA cells [can be] is configured to selectively enable the portion of peripheral functions (fig 1-3), wherein the FPGA cell [can be] is programmed to complete connections from one of the plurality of buses to the peripheral functions or tie the peripheral functions to an inactive state (fig 1-3), and wherein the FPGA cell is programmed through a register (col 5 lines 5-6, col 6 line 45+) coupled thereto.

(Claim 2) a bus (in fig 1-5) coupled to the at least one FPGA cell.

(Claim 3) wherein the FPGA cell (in fig 1-3) [can be] is programmed to complete connections from the bus to the peripheral functions or tie the peripheral function to an inactive state.

(Claims 4, 9) wherein the FPGA cell programs a register (col 5 lines 5-6, col 6 line 45+) coupled thereto.

(Claim 5) wherein a customer can configure the FPGA cell (fig 1-3).

(Claim 8) wherein the FPGA cell (fig 1-3) [can be] is programmed to complete connections from the bus (in fig 1-5) to the peripheral functions or tie the peripheral functions to an inactive state

(Claim 11) wherein the plurality of base functions comprise any combination of:

a processor, a universal interrupt controller, an SDRAM controller, an on-chip controller (OCM), an SRAM, a PLB arbiter, an OPB arbiter, an OPB bridge, and a UART (fig 2-4).

(Claim 12) wherein the plurality of peripheral functions comprise any combination of:

an external bus controller (EBC), an SDRAM controller, a proprietary function, a peripheral controller, an IsquareC Interface, a second UART, a DMA controller, a media access layer (MAL) function, and a plurality of media access controllers (MACs) (fig 2-4).

2. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al (US Patent Publication No 2002/0010902)

(Claim 1) a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions (fig 1-2); and

at least one FPGA cell, coupled to the plurality of peripheral functions, wherein the FPGA cell [can be] is configured to selectively enable the plurality of peripheral functions (fig 1-2).

(Claims 6-7) a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions (fig 1-2);

a plurality of buses (in fig 1-2) wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB); and

a plurality of FPGA cells (fig 1-2), each of the plurality of FPGA cells coupled to a portion of the peripheral functions and to one of the plurality of buses, wherein each of the plurality of FPGA cells [can be] is configured to selectively enable a number of peripheral functions.

(Claim 10) a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions (fig 1-2);

a plurality of buses (in fig 1-2), wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB), and

a plurality of FPGA cells (fig 1-2), each of the plurality of FPGA cells coupled to a portion of the peripheral functions and to one of the plurality of buses, wherein each of the plurality of FPGA cells [can be] is configured to selectively enable the portion of peripheral functions (fig 1-2), wherein the FPGA cell [can be] is programmed to complete connections from one of the plurality of buses to the peripheral functions or tie the peripheral functions to an inactive state (fig 1-2), and wherein the FPGA cell is programmed through a register (fig 2) coupled thereto.

(Claim 2) a bus (in fig 1-2) coupled to the at least one FPGA cell.

(Claim 3) wherein the FPGA cell (in fig 1-2) [can be] is programmed to complete connections from the bus to the peripheral functions or tie the peripheral function to an inactive state.

(Claims 4, 9) wherein the FPGA cell programs a register (in fig 2) coupled thereto.

(Claim 5) wherein a customer can configure the FPGA cell (fig 1-2).

(Claim 8) wherein the FPGA cell (fig 1-2) [can be] is programmed to complete connections from the bus to the peripheral functions or tie the peripheral functions to an inactive state

(Claim 11) wherein the plurality of base functions comprise any combination of:

a processor, a universal interrupt controller, an SDRAM controller, an on-chip controller (OCM), an SRAM, a PLB arbiter, an OPB arbiter, an OPB bridge, and a UART (fig 1-2).

(Claim 12) wherein the plurality of peripheral functions comprise any combination of:

an external bus controller (EBC), an SDRAM controller, a proprietary function, a peripheral controller, an IsquareC Interface, a second UART, a DMA controller, a media access layer (MAL) function, and a plurality of media access controllers (MACs) (fig 1-2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner

Paul Dinh
3/19/05